

What is claimed is:

1 1. A gate process for an embedded memory device,
2 comprising the steps of:

3 providing a semiconductor silicon substrate having a
4 memory cell area and a logic circuit area;

5 forming a first dielectric layer overlying the
6 semiconductor silicon substrate;

7 forming a gate structure overlying the first dielectric
8 layer of the memory cell area;

9 forming a protective layer overlying the first
10 dielectric layer and the top and sidewall of the
11 gate structure;

12 forming an insulating spacer overlying the protective
13 layer disposed overlying the sidewall of the gate
14 structure;

15 performing a pre-cleaning process to remove the
16 protective layer and the first dielectric layer
17 overlying the logic circuit area;

18 forming a second dielectric layer overlying the logic
19 circuit area; and

20 forming a gate layer overlying the second dielectric
21 layer of the logic circuit area.

1 2. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the memory cell area comprises a
3 flash memory cell or a DRAM cell.

1 3. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the first dielectric layer is a
3 silicon oxide layer.

1 4. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the gate structure overlying the
3 memory cell area comprises:

4 a floating gate layer formed overlying the first
5 dielectric layer of the memory cell area;
6 a dielectric structure formed overlying the floating
7 gate layer; and
8 a control gate layer formed overlying the dielectric
9 structure.

1 5. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the protective layer is a
3 silicon oxide layer or a silicon nitride layer.

1 6. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the protective layer has a
3 thickness of 50-500Å.

1 7. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the pre-cleaning process removes
3 the protective layer and the first dielectric layer disposed
4 outside the insulating spacer overlying the memory cell
5 area.

1 8. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the second dielectric layer is a
3 silicon oxide layer.

1 9. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the second dielectric layer is
3 formed overlying the memory cell area.

1 10. The gate process for an embedded memory device as
2 claimed in claim 1, wherein the formation of the gate layer
3 overlying the logic circuit area comprising the steps of:

4 depositing a conductive layer overlying the second
5 dielectric layer;
6 forming a first photoresist layer overlying the
7 conductive layer to cover the logic circuit area;
8 etching the conductive layer overlying the memory cell
9 area;
10 removing the first photoresist layer;
11 forming a second photoresist layer to cover the memory
12 cell area and has a pattern corresponding to the
13 gate layer overlying the logic circuit area;
14 removing the exposed conductive layer, in which the
15 conductive layer remaining overlying the logic
16 circuit area serves as the gate layer; and
17 removing the second photoresist layer.

1 11. A gate structure for an embedded memory device,
2 comprising:

3 a semiconductor silicon substrate having a memory cell
4 area and a logic circuit area;
5 a tunnel dielectric layer formed overlying the memory
6 cell area of the semiconductor silicon substrate;
7 a gate structure formed overlying the tunnel dielectric
8 layer of the memory cell area;

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9 a protective layer formed overlying the tunnel
10 dielectric layer and the sidewall of the gate
11 structure;
12 an insulating spacer formed overlying the protective
13 layer disposed overlying the sidewall of the gate
14 structure;
15 a gate dielectric layer overlying the logic circuit
16 area of the semiconductor silicon substrate; and
17 a gate layer formed overlying the gate dielectric layer
18 of the logic circuit area.

1 12. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the memory cell area
3 comprises a flash memory cell or a DRAM cell.

1 13. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the tunnel dielectric layer
3 is a silicon oxide layer.

1 14. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the gate structure overlying
3 the memory cell area comprises:

4 a floating gate layer formed overlying the first
5 dielectric layer of the memory cell area;
6 a dielectric structure formed overlying the floating
7 gate layer; and
8 a control gate layer formed overlying the dielectric
9 structure.

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1 15. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the protective layer is a
3 silicon oxide layer or a silicon nitride layer.

1 16. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the protective layer has a
3 thickness of 50~500Å.

1 17. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the gate dielectric layer is
3 a silicon oxide layer.

1 18. The gate structure for an embedded memory device
2 as claimed in claim 11, wherein the gate layer is a
3 polysilicon layer.

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